Tutorial Questions

1. Given the Boolean function

   F = xy'z + x'y'z + xyz

   a. List the truth table of the function
   b. Draw the logic diagram using the original Boolean Expression
   c. Simplify the algebraic expression using Boolean algebra
   d. List the truth table of the function from the simplified expression and show that it is the same as the truth table in part(a)
   e. Draw the logic diagram from the simplified expression and compare the total number of gates with the diagram of part(b)

2. A sequential circuit has two D flip flops A and B, two inputs x and y & one output z. The flip flop input equations & the circuit output as follows

   Da = x'y + xA

   Db = x'B+ xA

   Z =B

   a) Draw the logic diagram of the circuit
   b) Tabulate the state table

3. Show that a JK flip flop can be converted to a D Flip-Flop with an inverter between the J & K inputs.
4. Simplify the following function F together with the don't care condition d in (1) Sum of Products form (2) Product of Sums form

   F(w,x,y,z) = (2,3,4,5,6,7,11,14,15)

5. A Rom chip of 4096 X 16 bits will contain how many 128 X 8 memory chips.
6. The following memory units are specified by the no. of words times the number of bits per word. How many address lines and input-output lines are needed in each case. A) 2K X 16 b) 64K X 8 c) 16M X 32 d) 4G X 64
7. How many flip flops will be complemented in a 10 bit binary count to reach the next count after a) 1001100111 b) 0011111111

8. A ring counter is a shift register with the serial output connected to the serial input. Starting from an initial state of 1000 list the sequence of states of the four flip flops after each shift.
9. The content of a 4 bit register is initially 1101.The register is shifted 6 times to the right with the serial input being 101101 . what is the content of the register after each shift.
10. obtain the 9's complement of the following 8 digit decimal numbers.
    12349876 00980100 90009951 00000000
11. Represent the number +46.5 as a floating point binary number with 24 bits. The normalized fraction mantissa has 16 bits & the exponent has 8 bits.
12. perform the arithmetic operations (+70) + (+80) and (-70) + (-80) with binary numbers in signed 2's complement representation. Use eight bits to accommodate each number together with its sign. Show that overflow occurs in both cases & there is a sign reversal.
13. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is connected with multiplexers.
    a) How many selection input are there in each multiplexer.
    b) What size of multiplexers are needed.
    c) How many multiplexers are there in the bus.
14. Starting from an initial value of R = 11011101 determine the sequence of binary values in R after a logical shift left, followed by a circular shift right, followed by a logical shift right and a circular shift left.
15. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code , a register code part to specify one of 64 registers and an address part.
    a) How many bits are there in the operation code, the register code part and the address part.
    b) Draw the instruction code format and indicate the number of bits in each part.
16. Explain why each of the following microoperations cannot be executed during a single clock pulse.
    a) IR < - M[PC]
    b) AC < - AC + TR

c) DR <- DR+AC

17. Write a program to add & sbtract two numbers in IA-32 architecture format.
18. Perform the arithmetic operations below with binary numbers and with negative numbers in signed 2's complement representation. Use seven bits to accommodate each number together with its sign. In each case determine if there is an overflow by checking the carries into and out of the sign bit position.
    a) (+35) + (+40)
    b) (-35) + (-40)
    c) (-35) - (+40)
    d)(+35) - (+40)
19. Formulate a hardware procedure for detecting an overflow by comparing the sign of the sum with the signs of the augend and the addend. The numbers are in signed 2's complement representation.
20. Mark each individual path in the signed magnitude arithmetic flowchart by a number & then indicate the overall path that the algorithm takes when the following signed magnitude numbers are computed. In each case give the value of AVF. The left most bit in the following numbers represents the sign bit.
    a) 0 101101 + 0 011111
    b) 1 011111 + 1 101101
    c) 0 101101 – 0 011111
    d) 0 101101 - 0101101
    e) 1 011111 - 0 101101